What is claimed is

1. A method of forming a split gate field effect transistor, comprising:

providing a substrate having a pair of floating gates, a first conductive material layer between said pair of floating gates, and a first dielectric layer above said first conductive material layer;

forming a control gate having a second dielectric layer above said control gate, wherein said control gate is self-aligned to said pair of floating gates by using said first and second dielectric layers as an etching hard mask; and

forming a pair of source/drain regions into said substrate and beside said pair of floating gates and said control gate.

2. The method of claim 1, wherein each of said first dielectric layer and said second dielectric layer comprises a silicon oxide layer.

3. The method of claim 2, wherein said second dielectric layer is formed by a method of thermal oxidation.

4. The method of claim 2, wherein said silicon oxide layer has a thickness from about 50 angstroms to about 400 angstroms.

5. The method of claim 1, wherein said second dielectric layer is thicker at a middle portion than at an edge portion.

6. The method of claim 1, wherein said step of forming said control gate comprises:

forming a second conductive material layer above said substrate;

forming a hard mask layer above said second conductive material layer;

removing portions of said hard mask layer and said second conductive material layer;

forming said second dielectric layer above said second conductive material layer; and

removing a remaining portion of said hard mask layer and an additional portion of said second conductive material layer by using said first dielectric layer and said second dielectric layer as said etching hard mask.

7. The method of claim 6, wherein said second dielectric layer is formed by using said hard mask layer as an oxidation resistant layer.

8. The method of claim 7, wherein said hard mask layer comprises a silicon nitride layer.

9. The method of claim 6, wherein said step of removing portions of said hard mask layer and said second conductive material layer comprises:

forming a sacrificial layer above said hard mask layer;

removing portions of said sacrificial layer, said hard mask layer and said second conductive material layer;

removing a remaining portion of said sacrificial layer;

10. The method of claim 9, wherein said sacrificial layer is used to planarize a surface of said substrate

11. The method of claim 10, wherein said sacrificial layer comprises an organic material layer.

12. The method of claim 11, wherein said organic material layer comprises a photoresist.

13. The method of claim 10, wherein said sacrificial layer comprises a spin-on glass layer.

14. A split gate field effect transistor, comprising:

a substrate;

a gate dielectric layer formed above said substrate;

a floating gate formed above said gate dielectric layer;

an inter-gate dielectric layer formed above said floating gate;

a substantially rectangular control gate formed above said inter-gate dielectric layer, wherein a dielectric layer is formed above said control gate and said control gate is offset said floating gate; and

a pair of source/drain regions formed into said substrate and beside said floating gate and said substantially rectangular control gate.

15. The split gate field effect transistor of claim 14 wherein said substantially rectangular control gate does not overlay said floating gate.

16. The split gate field effect transistor of claim 14 wherein said substantially rectangular control gate has a concave top surface.

17. The split gate field effect transistor of claim 14 wherein said substantially rectangular control gate is formed by using a dielectric layer above said substantially rectangular control gate as an etching hard mask.

18. The split gate field effect transistor of claim 14, wherein said dielectric layer comprises a silicon oxide layer.

19. The split gate filed effect transistor of claim 18, wherein said silicon oxide layer is formed by a method of thermal oxidation.

20. The split gate field effect transistor of claim 18, wherein said silicon oxide layer has a thickness from about 50 angstroms to about 400 angstroms.

21. The split gate field effect transistor of claim 17, wherein said dielectric layer is thicker at a middle portion than at an edge portion.

22. A structure for forming a split gate effect transistor, comprising:

a substrate having a pair of floating gates, a first conductive material layer between said pair of floating gates, and a first dielectric layer above said first conductive material layer;

a second conductive material layer formed above said substrate;

a hard mask layer formed above said second conductive material layer; and

a sacrificial layer formed above said hard mask layer.

23. The structure of claim 22, wherein said sacrificial layer is used to planarize a surface of said substrate.

24. The structure of claim 23, wherein said sacrificial layer comprises an organic material layer.

25. The structure of claim 24, wherein said organic material layer comprises a photoresist.

26. The structure of claim 23, wherein said sacrificial layer comprises a spin-on glass layer.

27. The structure of claim 22, wherein said hard mask layer comprises an oxidation resistant layer.

28. The structure of claim 27, wherein said oxidation resistant layer comprises a silicon nitride layer.

29. The structure of claim 22, wherein said first dielectric layer has a thickness from about 50 angstroms to about 400 angstroms.

30. The structure of claim 22, wherein said second conductive material layer completely covers said pair of floating gates and said first dielectric layer, said hard mask completely covers

said second conductive material layer, and said sacrificial layer completely covers said hard mask layer.

31. The structure of claim 22, wherein said second conductive material layer, said hard mask layer, and said sacrificial layer are offset from said pair of floating gates and said first conductive material layer

32. The structure of claim 31, wherein said second conductive material layer and said hard mask layer have a cross-section formed in substantially L shape.

33. The structure of claim 32, wherein said sacrificial layer contacts with two surfaces of said L shape of said hard mask layer.